CLAIMS

1. A method for testing circuitry in an FPGA, comprising:

configuring the FPGA for test including the FPGA forming an FPGA scan chain for simulating an external connection to an embedded device;

receiving and conducting at least one device scan chain to the embedded device; and

performing test.

2. The method of claim 1 further including isolating the embedded device.

3. The method of claim 1 further including transmitting at least one test signal to a multiplexer for delivery to the embedded device.

4. The method of claim 1 further including receiving at least one test output signal from a multiplexer coupled to receive at least one output from the embedded device.

5. The method of claim 4 further including storing the at least one test output signal in the FPGA scan chain.

6. The method of claim 5 further including the step of receiving at least one device scan chain from the embedded device, which at least one scan chain includes test output signals from within the embedded device.

7. The method of claim 6 further including transmitting the at least one device scan data through the FPGA fabric to an external tester for evaluation.

8. The method of claim 5 further including outputting

scan data through FPGA scan chain to an external tester for evaluation.

9. A method for testing an FPGA, comprising:

configuring the FPGA for test;

transmitting a test signal to a multiplexer formed within a gasket; and

transmitting the test signal from the multiplexer to a device under test.

10. The method of claim 9 wherein the device under test is an embedded core device.

11. The method of claim 9 wherein the device under test is a fixed logic device formed within the gasket.

12. The method of claim 9 wherein the step of configuring the FPGA for test includes receiving an FPGA scan chain with test vectors.

13. The method of claim 9 further including, if the device under test is an embedded core device, receiving and conducting at least one device scan chain to the device under test.

14. A method for testing an FPGA, comprising:

configuring the FPGA for test;

transmitting an output test signal from a device under test to a multiplexer formed within a gasket; and

transmitting the output test signal from the multiplexer to an FPGA fabric portion.

15. The method of claim 14 wherein the device under test is an embedded core device.

16. The method of claim 14 wherein the device under

test is a fixed logic device formed within the gasket.

17. The method of claim 14 wherein the step of configuring the FPGA for test includes outputting an FPGA scan chain with test vectors to an external tester.

18. The method of claim 14 further including, if the device under test is an embedded core device, receiving at least one device scan chain from the device under test and conducting the at least one device scan chain through an FPGA fabric portion to an external tester for evaluation.

19. A method for testing an embedded fixed logic core device, comprising:

receiving, at a multiplexer, one of a device ID signal from an ID storage module or a test signal from a test circuit;

receiving, at the multiplexer, a control signal; and

responsive to the control signal, transmitting either the device ID signal or the test signal to the embedded fixed logic core device.

20. An FPGA, comprising:

an FPGA fabric portion;

a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion; and

at least one multiplexer coupled serially between the FPGA fabric portion and the embedded core device.

21. The FPGA of claim 20 wherein the multiplexer is coupled to receive outputs from a fixed logic device formed within the gasket.

22. The FPGA of claim 21 wherein the multiplexer is coupled to receive test signals from the FPGA fabric portion

by way of communication paths formed within the Gasket portion, which communication paths are accessible while the FPGA is configured for testing the embedded device.

23. The FPGA of claim 22 wherein the multiplexer couples the test signals received from the FPGA fabric portion to the embedded core device whenever the FPGA is configured for testing the embedded device.

24. The FPGA of claim 20 wherein the multiplexer is coupled to receive outputs from the embedded core device.

25. The FPGA of claim 20 wherein the multiplexer is coupled to produce received outputs to the FPGA fabric portion by way of communication paths formed within the Gasket portion, which communication paths are accessible while the FPGA is configured for testing the embedded device.

26. The FPGA of claim 20 wherein the multiplexer is coupled to produce received outputs from the embedded core device to fixed logic circuit formed within the Gasket whenever the FPGA is not configured for testing.